9. (NEW) A method using an array processor for frame rendering and DSP applications, comprising:

determining a fixed point result by performing a fixed point addition or subtraction on a plurality of fixed point operands;

converting the fixed point result to a first floating point result; and

determining a second floating point result by performing a floating point multiplication and then accumulation on the first floating point result and a plurality of floating point operands.

REMARKS

Rejections under 35 U.S.C. §102(b)

Claims 1-3 were rejected under 35 U.S.C. §102(b) as being anticipated by Arambepola, USPN 4,879,559. We respectfully traverse the rejections.

Arambepola has an processing unit sections (37) of processing unit 31, consisting of a plurality of MAC's (43) and a "Range Migration Interpolator" (45) (Figs. 6 and 7, col. 4, lines 54-64). From Fig. 6a the processing unit sections (37) of processing unit 31 are inter-linked by mux 72 (col. 7, lines 50-58). In addition, from Figs. 6 and 6a, a single operand is not shared by the MAC's (43).

Claim 1 has been amended to further described the array processor (Fig. 2). A first multiply/accumulator (MAC) unit coupled to a first local memory, the first local memory having a first plurality of operands; a second MAC unit coupled to a second local memory, the second local memory having a second plurality of operands; and a shared operand unit coupled to the first MAC unit and the second MAC unit for providing a shared operand to the first MAC unit for computing a first result in association with the first plurality of operands and to the second MAC unit for computing a second result in association with the second plurality of operands; and wherein the first result and the second result are computed independently of each other.

Thus the processing unit sections (e.g., 900 and 920) in claim 1 work independently, unlike Arambepola where each processing unit (37) needs input from some adjacent processing unit. Thus claim 1 should be allowable for at least this reason.

Claims 2 and 3 being dependent on claim 1 should be allowable for at least the same reason claim 1 is allowable.

Rejections under 35 U.S.C. §103(a)

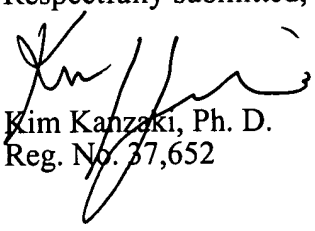
Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over Arambepola, USPN 4,879,559. We respectfully traverse this rejection. The Examiner assumes the wire bundle between the MAC's (43) and the N to 1 Mux (46) is what is referred to in claim 4. This is not correct, in claim 4 the wire bundle is between the interface and the array processor. However, even assuming for the sake of argument, the wire bundle could be N wires, in col. 10, lines 13 – 19, N is less than or equal to 10. Thus it is not obvious according to the specification that N be at least 256. Thus for at this reason claim 4 should be allowable.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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